University of Jordan

Computer Engineering Department

CPE234: Digital Logic Lab

Spring Semester 2013-2014

COURSE OUTLINE

Instructors	Dr.Khalid Darabkeh (Coordinator), Eng.Saadeh Sweadan, Eng.Asma Abdelkarim, Eng.Ola Al-Jaloudy, Eng.Amal Quzmar, Eng.Rawan Al-Jamal, Eng. Fatima Al-Qudah.
Home page	http://logic-ju.ucoz.com/
No. of credit hrs	1
Pre-Requisites	CPE 231
Lab Description	Experiments on basic TTL and CMOS logic gates, including simulations to explore functionality and timing parameters. Experiments using both simulation and practical hardware implementation on CPLDs or FPGAs, using VHDL for combinational and sequential circuits including multiplexers, demultiplexers, decoders, encoders, shift registers, counters, latches and memory. Experiments in logic design using state machines.
Textbook	The Lab has a set of experiments that will be posted on the website of the lab.
Grading	Mid Practical Lab Exam: 30% In-Lab Reports: 15% Quizzes: 15% Final Exam: 40%

Starting Date	**Experiments Description**
16/2	Lab Preparations.
23/2	Distribution of Lab Syllabus+Basic Logic Gates Implementation Using Bread boards and Discrete Gates.
2/3	Introduction to Altera and schematic programming using Quartus II software.
9/3	Introduction to Verilog programming using Quartus II Software.
16/3	Combinational Circuits Design Using Verilog & Implementations in FPGAs, **Quiz 1 (7 marks)**
23/3	Decoder/Encoder Applications.
30/3	**Midterm Exam.**
6/4	Multiplexers/Demultiplexers Design and Implementation (Time Division Multiplexing).
13/4	Arithmetic Circuits Design and Implementation (2-bit ALU)
20/4	Latches, Flip-Flops, Registers and Counters applications , **Quiz 2 (8 marks)**
27/4	
4/5	Memory Design

Final Exam 28/5/2014

References	• Logic and Computer Design Fundamentals and Xilinx Student Edition 4.2 Package, M. Morris Mano and Charles R. Kime (4th edition, 2008). Prentice Hall. • Altera DE2 Development and Education Board User Manual. • A Simple Design in VHDL Using Altera Quartus II 6.1 Web Edition.
Expected Outcomes	Upon completion of this course, a student should: • Implement the concepts learned in the digital logic course with Altera. • Become familiar with digital lab equipments, breadboards, wiring and 7400 logic chips. • Conduct experiment with logic circuits in SOP and POS form using discrete TTL logic gates. • Conduct experiment by synthesizing, verifying and implementing combinational digital circuits. • Conduct experiment by designing, simulating and implementing a counter and/or a shift register. • Practice teamwork to complete a design project. • Earn the skill to document the lab work in a technical report.
Guidelines	• No makeups are allowed under any circumstances for either exams or quizzes. • All mobile phones must be turned off during the lab. • Cheating will not be tolerated. • All work must be yours. • Two absents are maximally allowed. • Quizzes will reflect your understanding for previous experiments and your preparing for new experiment. • Quizzes will start at the beginning of lab Time.