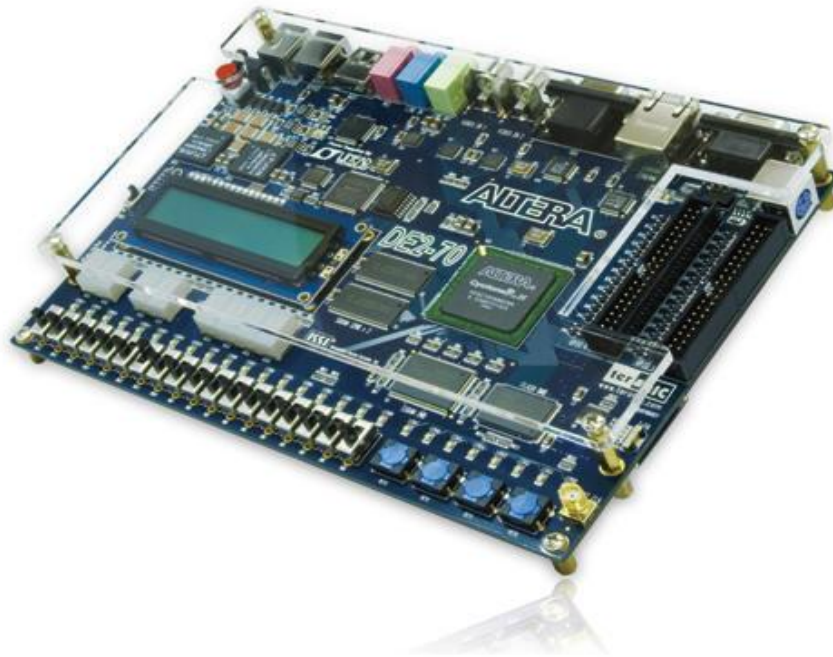




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Labsheet 7: Latches and Flip-Flops

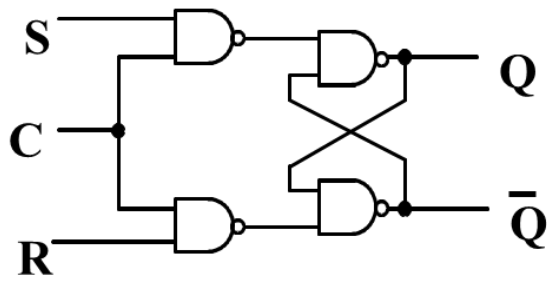


Name:

Student ID:

Section:

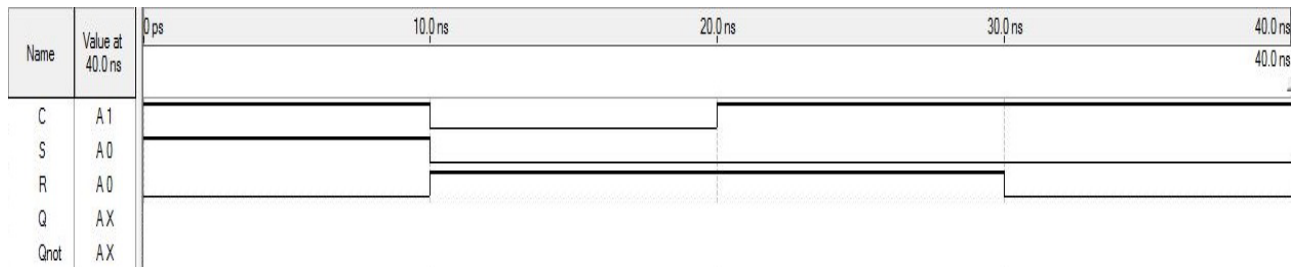
Part 1: Clocked SR-latch Verilog implementation and simulation:



SR-Latch Function table

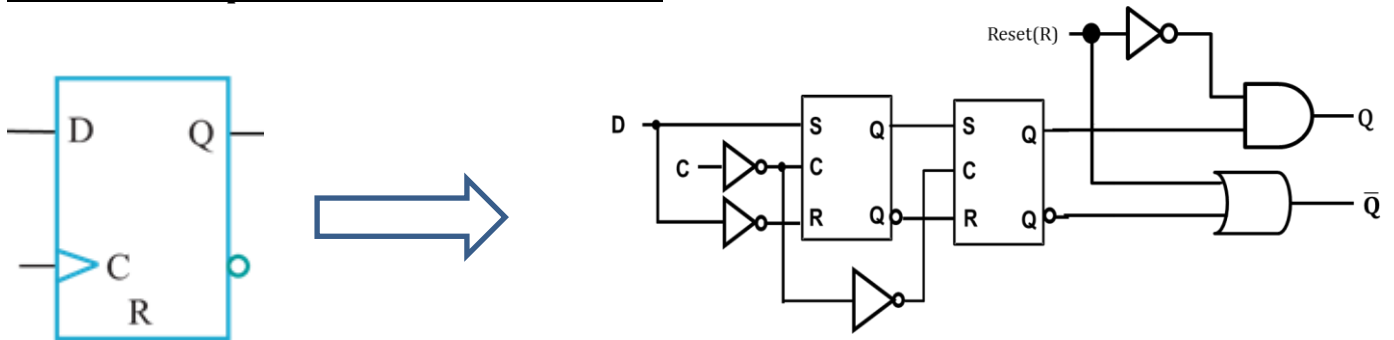
C	S	R	operation
0	x	x	Hold
1	0	0	Hold
1	0	1	Reset
1	1	0	Set
1	1	1	Forbidden

1. By hand, complete the below timing diagram for the clocked SR-latch.



- Inside **SR2.v** file, write a structural Verilog module to implement the clocked SR-latch. Note: NAND gatmodules are already available in **lib.v** file
- Use the vector waveform file to perform a functional simulation for your module in SR2.v. Use the same input values as the above timing diagram in your simulation. Also, compare your simulation output to your output in above.

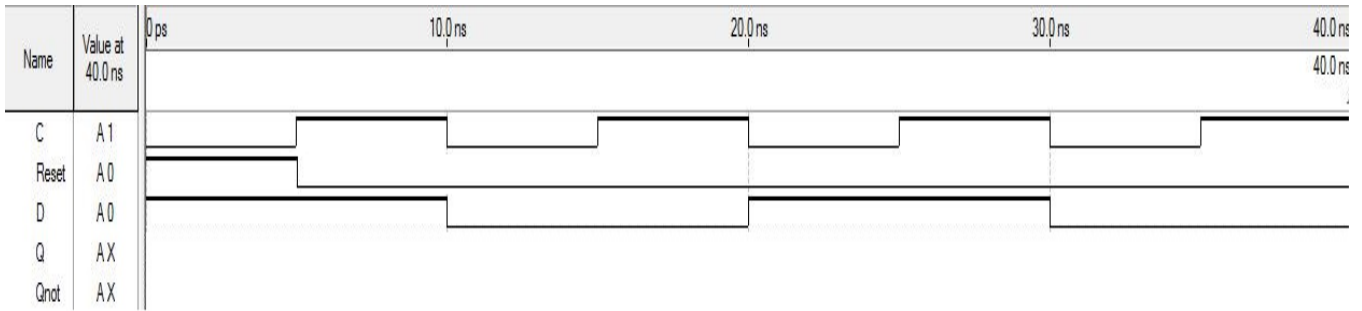
Part 2: D-FF implementation and simulation:



1. Fill the function table in below for the positive-edge triggered D-FF.

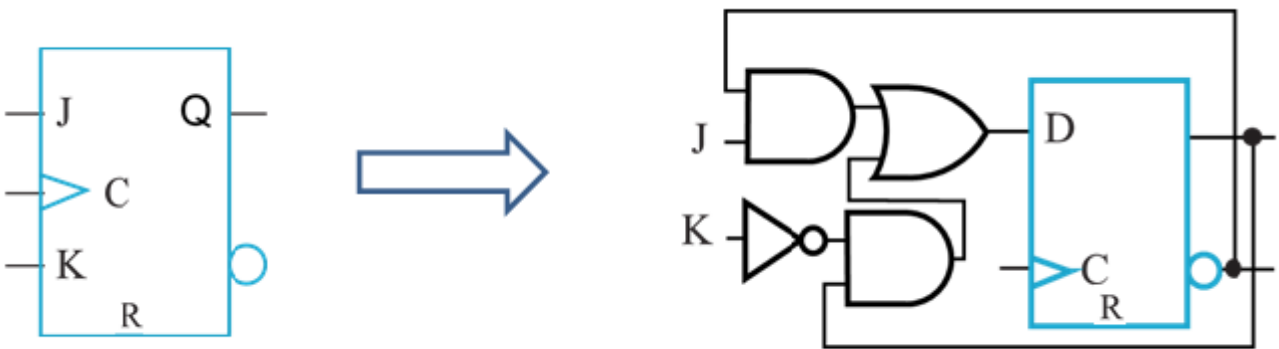
R	C	D	operation
1	x	x	
0	↑	0	
0	↑	1	

2. By hand, complete the below timing diagram for the D-FF.



- Inside `dff1.v` file, write a structural Verilog module to implement the D-FF circuit.
Note: You need to use the clocked SR-latch module defined in `SR2.v` and the basic gate modules defined in `lib.v`.
- Use the vector waveform file to perform a functional simulation for your module in `jkff1.v`. Use the same input values as the above timing diagram in your simulation. Also, compare your simulation output to your output in above.

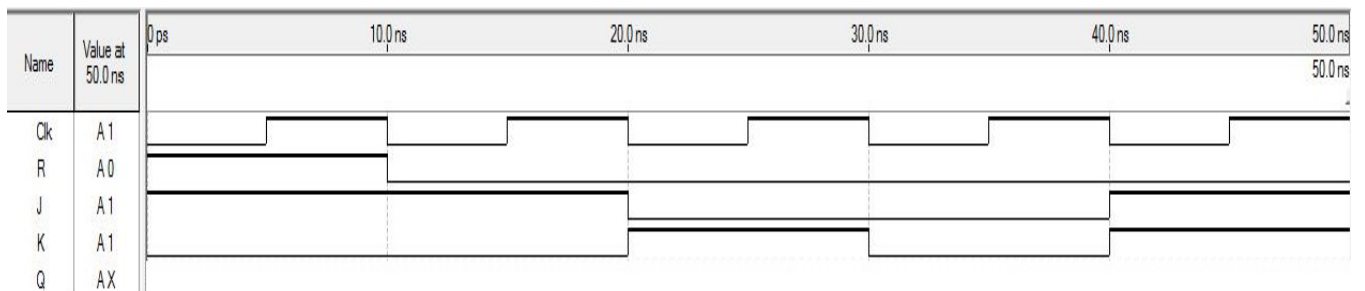
Part 3: JK-FF implementation and simulation:



1. Fill the function table in below for the positive-edge triggered JK-FF.

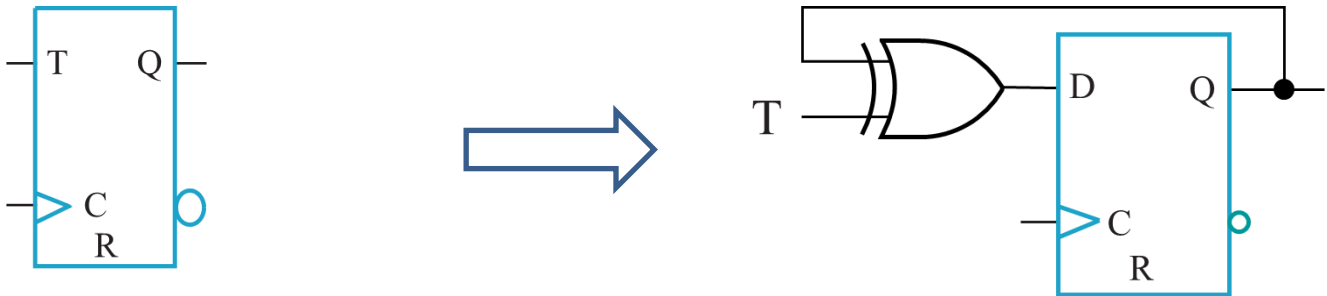
R	C	J	K	operation
1	x	x	x	
0	↑	0	0	
0	↑	0	1	
0	↑	1	0	
0	↑	1	1	

2. By hand, complete the below timing diagram for the JK-FF



- Inside `jkff1.v` file, write a structural Verilog module to implement the JK-FF circuit.
Note: You need to use the D-FF module defined in `dff1.v` and the basic gates modules defined in `lib.v`.
- Use the vector waveform file to perform a functional simulation for your module in `dff1.v`. Use the same input values as the above timing diagram in your simulation. Also, compare your simulation output to your output in above.

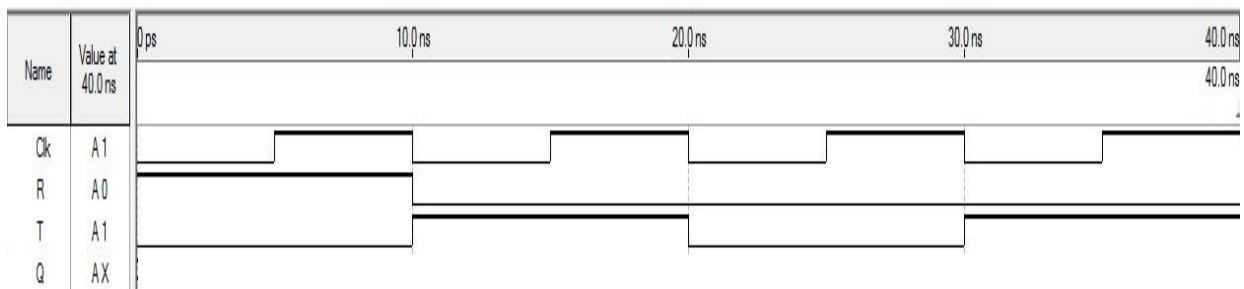
Part 4: T-FF implementation and simulation:



- Fill the function table in below for the positive-edge triggered T-FF.

R	C	T	operation
1	x	x	
0	↑	0	
0	↑	1	

- By hand, complete the below timing diagram for the T-FF



- Inside `tff1.v` file, write a structural Verilog module to implement the T-FF circuit.
Note: You need to use the D-FF module defined in `dff1.v` and the XOR module defined in `lib.v`.
- Use the vector waveform file to perform a functional simulation for your module in `tff1.v`. Use the same input values as the above timing diagram in your simulation. Also, compare your simulation output to your output in above.